IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of optimizing at least two target machines, comprising the steps of:

abstracting a rule of instruction scheduling for each of said at least two target machines;

generating a hypothetical machine based on said rule of instruction scheduling for each of said at least two target machines instructions; and targeting said hypothetical machine.

- 2. (Currently amended) The method of claim 1 wherein a <u>different</u> rule of instruction scheduling for said hypothetical machine is a restrictive set of said abstracted rules <u>rule</u> of instruction scheduling <u>for each</u> of said at least two target machines.
- (Currently amended) The method of claim 1 further including the steps of:
 detecting a conflict between said <u>rule of instruction scheduling for each of said at</u>
 least two target machines abstracted rules of instructions; and
 resolving said conflict.

- 4. (Currently amended) The method of claim 3 wherein said step of resolving said conflict includes the <u>a</u> step <u>of</u> selecting the <u>a</u> less damaging option <u>for</u> of said detected conflict.
- 5. (Currently amended) The method of claim 3 wherein said detected conflict corresponds to [[a]] an inherent conflict between said rule of instruction scheduling for each of said at least two target machines a rule of instruction of one of said at least two target machines.
- 6. (Original) The method of claim 1 further including the steps of: modeling each of said at least two target machines; and retrieving scheduling information corresponding to each of said at least two target machines.
- 7. (Original) The method of claim 1 wherein said at least two target machines include an UltraSPARC-II configured to operate at a speed of 360 MHz and an UltraSPARC-III configured to operate at a speed of 600 MHz.
- 8. (Currently amended) A method of optimizing at least two target machines, comprising the steps of:

retrieving scheduling information corresponding to each of said at least two target machines;

abstracting a rule of instruction scheduling for each of said at least two target machines;

PATENT

Appl. No. 09/823,207

Amdt. dated September 16, 2004

Reply to Office action of June 16, 2004

generating a hypothetical machine based on said rule of <u>instruction scheduling for</u>

<u>each of said at least two target machines</u> <u>instructions</u>; and

targeting said hypothetical machine.

9. (Currently amended) The method of claim 8 further including the steps of:

detecting a conflict between said rule of instruction scheduling for each of said at

least two target machines abstracted rules of instructions; and

resolving said conflict.

10. (Currently amended) The method of claim 9 wherein a different rule of

instruction scheduling for said hypothetical machine is a restrictive set of said rule

abstracted rules of instruction scheduling for each of said at least two target machines.

11. (Currently amended) The method of claim 9 wherein said step of resolving

said conflict includes the a step of selecting the a less damaging option for of said detected

conflict.

12. (Currently amended) The method of claim 9 wherein said detected conflict

corresponds to [[a]] an inherent conflict between [[a]] said rule of instruction for each of

said at least two target machines of one of said at least two target machines and a rule of

instruction of another of said at least two target machines.

13. (Currently amended) An apparatus for optimizing at least two target

machines, comprising:

means for abstracting a rule of instruction scheduling for each of said at least two target machines;

means for generating a hypothetical machine based on said rule of <u>instruction</u>
scheduling for each of said at least two target machines instructions; and
means for <u>targeting target</u> said hypothetical machine.

- 14. (Currently amended) The apparatus of claim 13 wherein a <u>different</u> rule of instruction scheduling for said hypothetical machine is a restrictive set of said <u>rule</u> abstracted rules of instruction scheduling <u>for each</u> of said at least two target machines.
- 15. (Currently amended) The apparatus of claim 13 further including:

 means for detecting a conflict between said <u>rule of instruction scheduling for each</u>

 of said at least two target machines abstracted rules of instructions; and

 means for resolving said conflict.
- 16. (Currently amended) The apparatus of claim 15 wherein said resolving means includes means for selecting the <u>a</u> less damaging option for of said detected conflict.
- 17. (Currently amended) The apparatus of claim 15 wherein said detected conflict corresponds to [[a]] an inherent conflict between said rule of instruction scheduling for each of said at least two target machines a rule of instruction of one of said at least two target machines and a rule of instruction of another of said at least two target machines.
 - 18. (Original) The apparatus of claim 13 further including: means for modeling each of said at least two target machines; and

means for retrieving scheduling information corresponding to each of said at least two target machines.

19. (Currently amended) An apparatus for optimizing at least two target machines, comprising:

means for retrieving scheduling information corresponding to each of said at least two target machines;

means for abstracting a rule of instruction scheduling for each of said at least two target machines;

means for generating a hypothetical machine based on said rule of <u>instruction</u>
scheduling for each of said at least two target machines instructions; and
means for targeting said hypothetical machine.

20. (Currently amended) An apparatus for optimizing a plurality of target machines, comprising:

means for modeling a plurality of target machines;

means for retrieving scheduling information corresponding to each of said plurality of target machines;

means for abstracting a rule of instruction scheduling for each of said plurality of target machines;

means for generating a hypothetical machine based on said rule of <u>instruction</u> scheduling for each of said plurality of target machines instructions;

means for target said hypothetical machine;

means for detecting a conflict between said <u>rule of instruction scheduling for each</u>
of said plurality of target <u>machines</u> abstracted rules of instructions; and

PATENT

Appl. No. 09/823,207 Amdt. dated September 16, 2004 Reply to Office action of June 16, 2004

means for resolving said conflict.